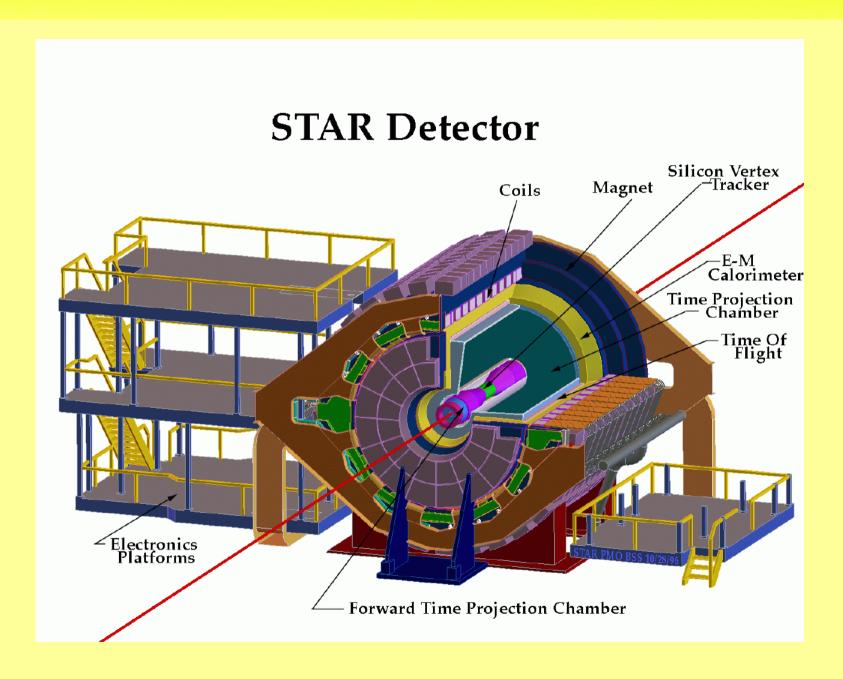
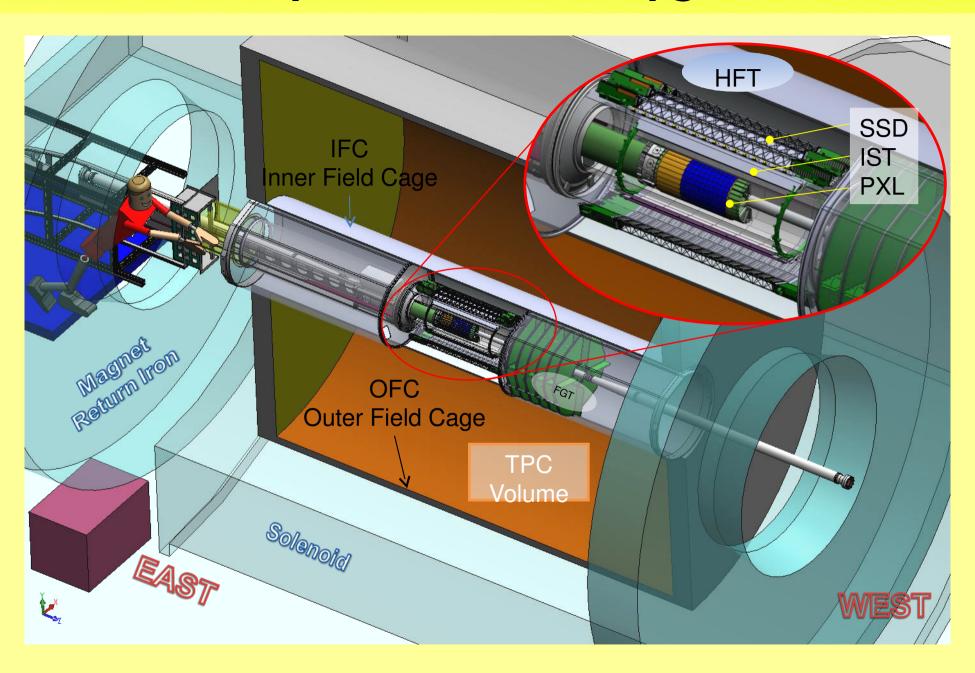
The STAR Heavy Flavor Tracker upgrade

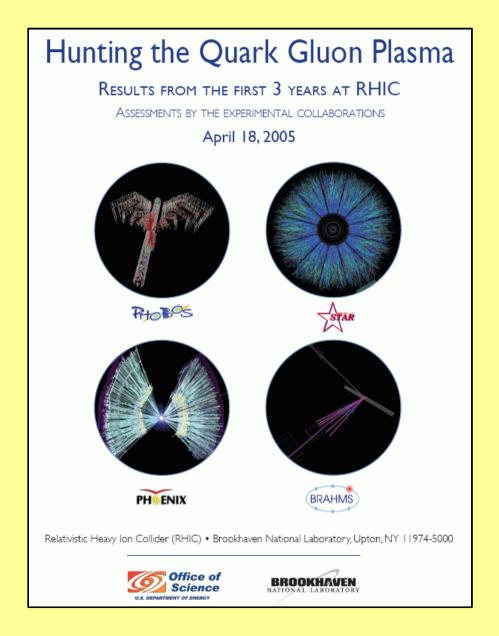
STAR

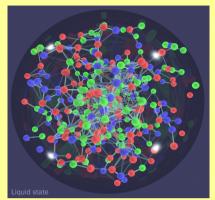


Heavy Flavor Tracker Upgrade



RHIC/Physics





T ~ 200-400 MeV

 $\varepsilon \sim 30-60 \, \varepsilon_{\text{nucl}}$

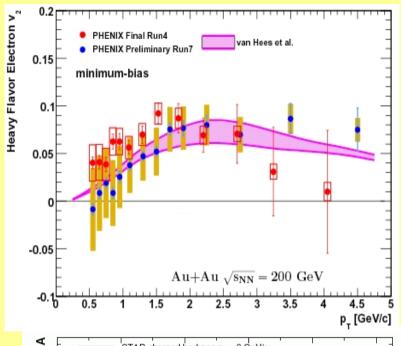
Perfect liquid

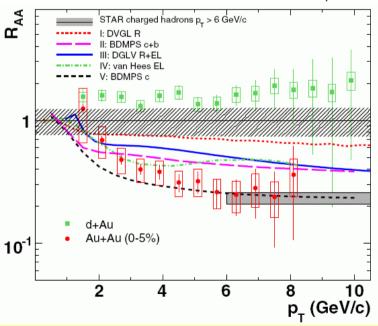
Flows as a relativistic quantum liquid with viscosity to energy density ratio lower than any other known liquid

Highly opaque to colored probes, quarks and gluons, but not to photons

Produces mesons and baryons with yield ratios and flow that suggests formation through quark coalescence from a hot thermal bath

RHIC/Physics/Puzzles





Non zero elliptic flow of electrons from heavy quark decay

Indicative for early thermalization

Expect significant Bottom contribution

Need direct topological reconstruction of heavy quark hadrons

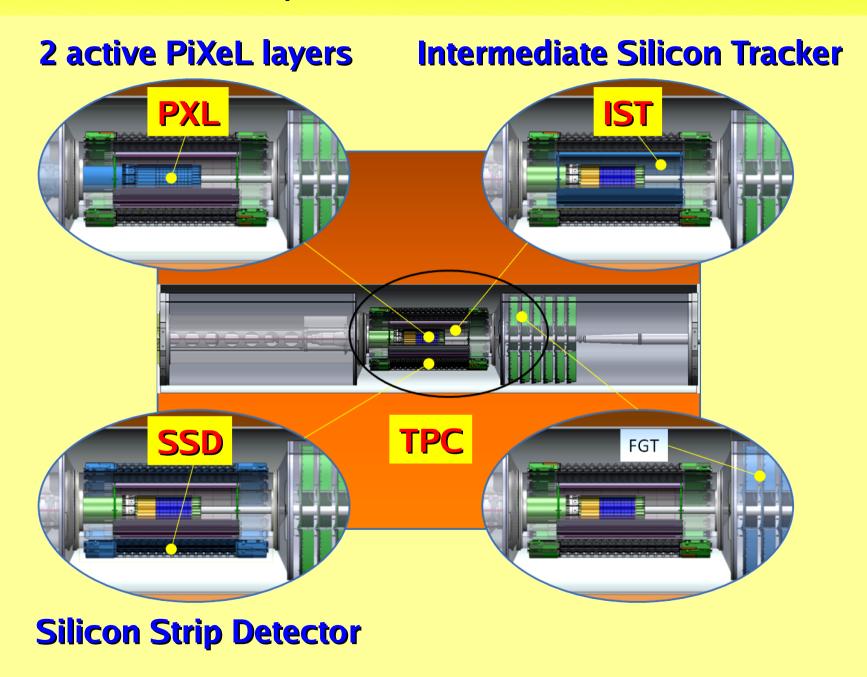
Suppression of electrons from heavy quark decay

Same as for light hadrons >6Gev/c

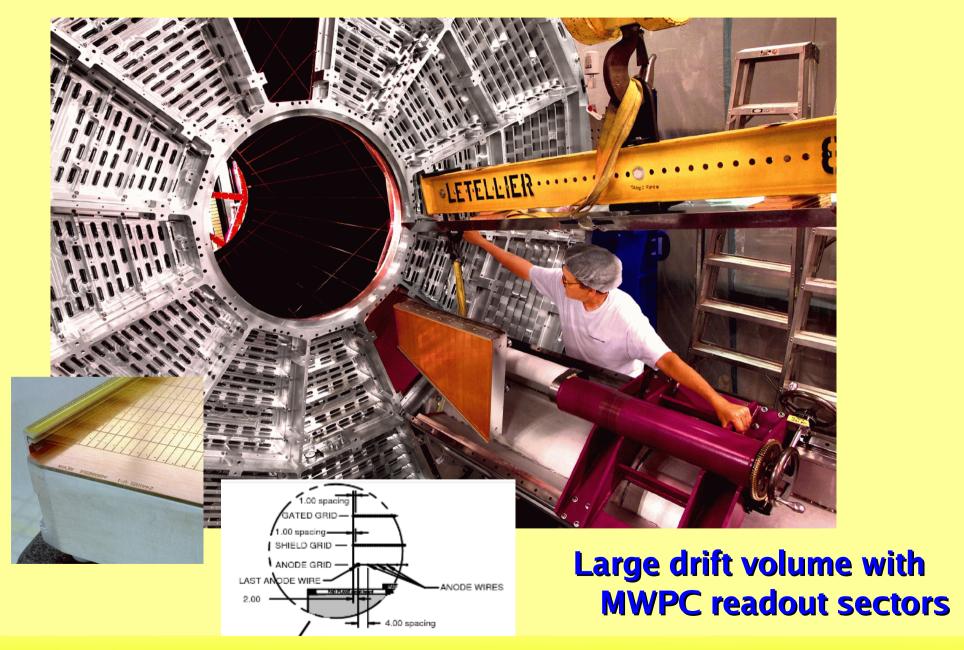
Heavy quark in-medium energy loss?

Need direct topological reconstruction of heavy quark hadrons

HFT/Detector

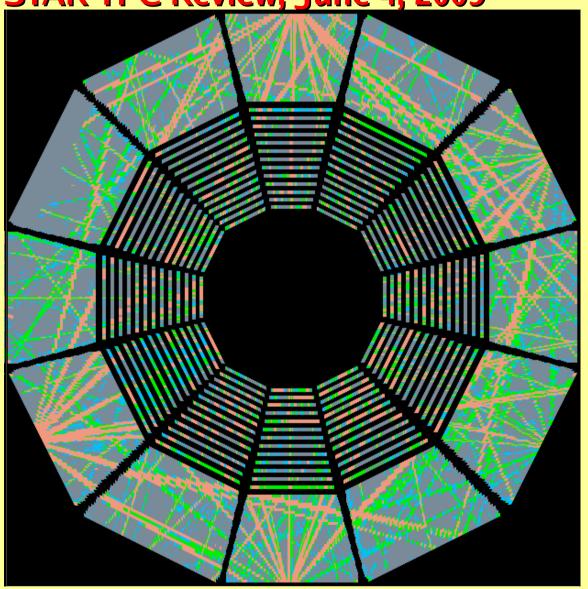


TPC



TPC/RHICII

STAR TPC Review, June 4, 2009



Jim Thomas

- Luminosity is up a factor of 3 compared to 2008 pp200 run, and expected to go up 4x in coming years
- Trigger rates can now go up a factor of 3 or more
- pp500 Multiplicities are
 1.25x higher than in pp200
- So we are working with ~5x more charge in the TPC than ever before and STAR may ask for ~40x before we are done

TPC/TipToeing towards RHICII

The STAR TPC is an indispensable 'work horse' for the HFT

Run9: many anode trips due to too much charge and high trigger rates

- leads to unacceptable recovery downtime
- long term wire aging
- short term electronics failures

Mitigation:

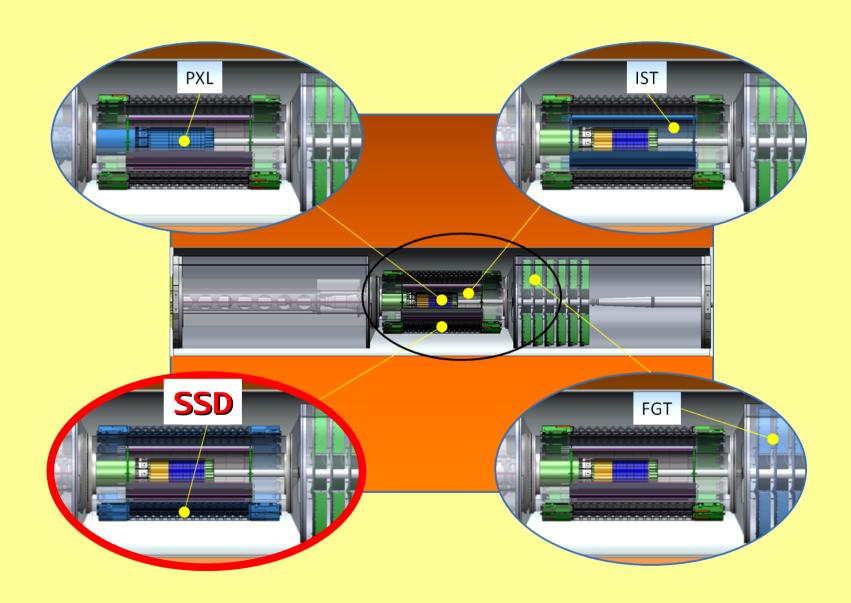
- Reduce the gain by 2/3, no negative effect because new electronics has increased S/N from 20:1 to 30:1
- Limit the trigger rate
- Limit the luminosity

Real future meltdown:

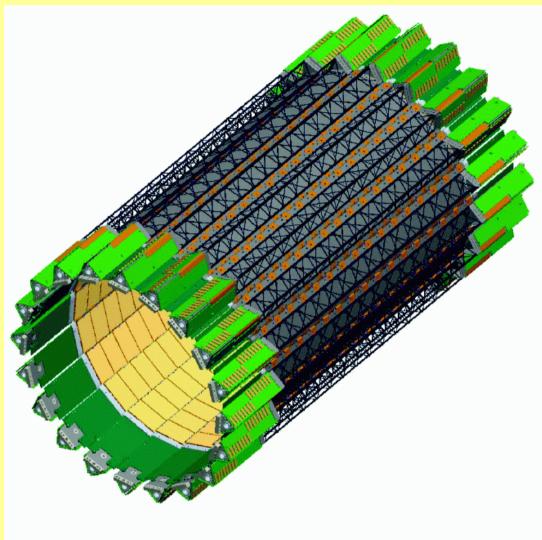
- Switch off inner sectors (and let SSD and IST take over)
- Replace anode wires (can be done at high cost)
- Replace MWPC technology by GEM (even higher cost and R&D)

We must choose which options to pursue with care and wisdom

HFT/SSD



HFT/SSD/Specifications



SSD Radius	22 cm
SSD Sensitive Length	67 cm
lηl coverage	< 1.2
Number of ladders	20
Number of wafers/ladder	16
Total # of wafers	320
# of strips/wafer side	768
# of sides/wafer	2
Total # of channels	491520
Silicon wafer size	$75 \times 42 \text{ mm}$
Silicon wafer sensitive size	$73 \times 40 \text{ mm}$
Silicon thickness	300 μm
Strip pitch	95 μm
Stereo Angle	35 mrad
r-φ resolution	20 μm
<u>z</u> resolution	740 µm

HFT/SSD/Improvements

Make readout speed compliant with DAQ1000

- parallelize digitization
- increase sampling speed
- increase data transfer speed and use buffers
- → 9% dead at 500Hz (old dead time ~ 60—70%)

Tiling instead of castellating the ladders

- improves hermiticity
- all ladders at same radius and tilt angle
- simplifies mechanical design

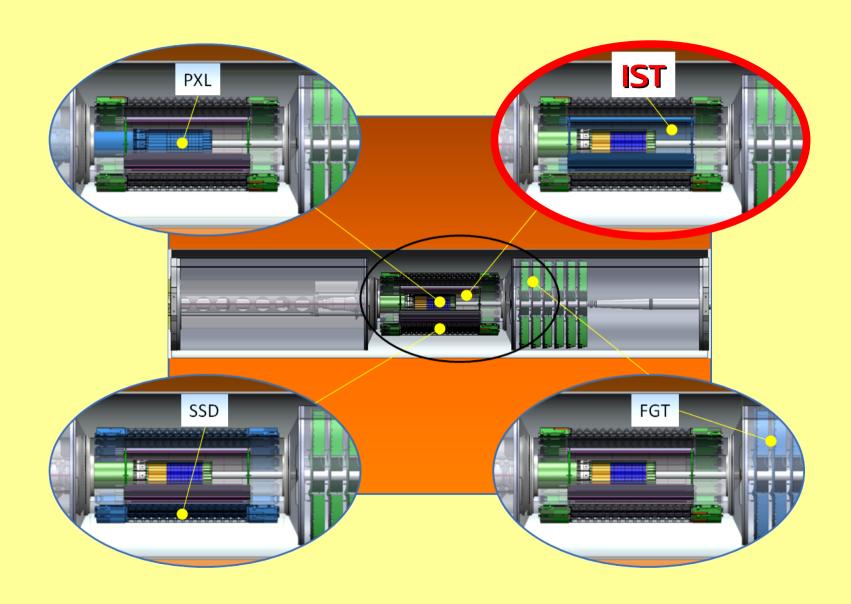
Improve reliability of air cooling

- use more rigid air lines to prevent squashing
- air suction from East side only
- use higher capacity 'vacuum cleaner'

SSD easily survives >10 years of 500GeV p+p

- 3.5 krad/year for 500GeV p+p at R=22cm
- rad limit is about 200 krad, mainly readout chip

HFT/IST



HFT/IST/Overview

Acceptance:

σ -1.2 < η < + 1.2 (97.8% spatial coverage)

Radiation length:

< 1.5%

Readout speed:

Resolve RHIC beam bunch crossing (107ns)

Radiation load:

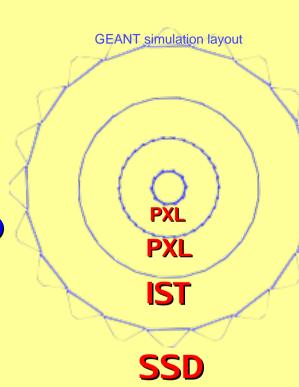
Survive 10 years of RHIC operation:

~30kRad/year

Hit requirements:

< 2% occupancy</p>

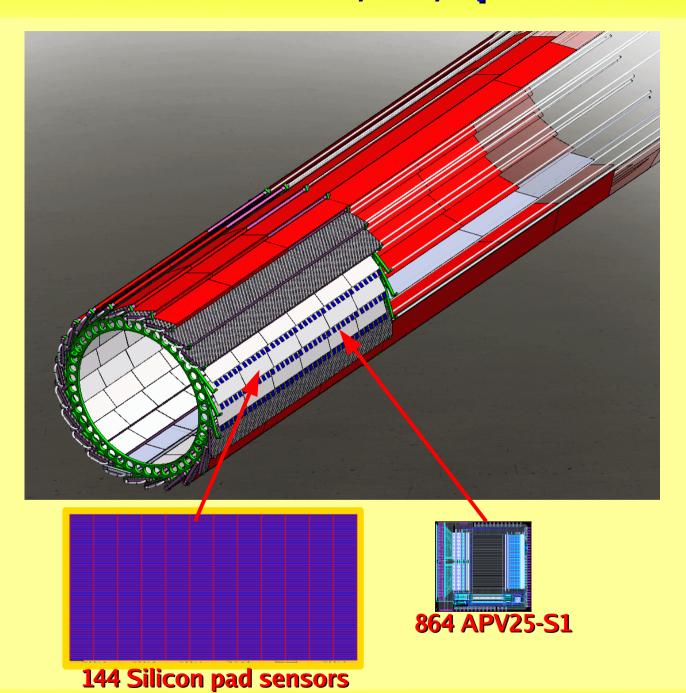
< 1% double hit probability</p>



TPC

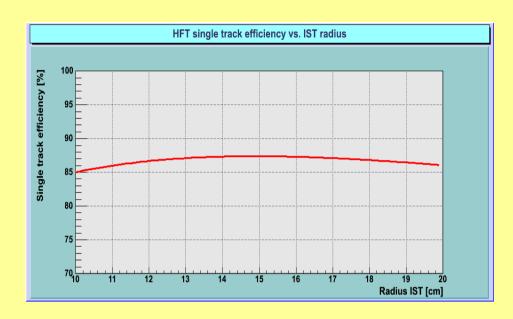
- 1-layer IST system
- Conservative choice of complete layout
- Hybrid: Kapton-based /
 Carbon-fiber support material
- Ladders: Profit from ATLAS experience
- Sensors: Silicon pad sensors Well proven technology and understood / LNS experience
- FEE: Based on APV25-S1 chip
 Basic Hybrid design exists
- DAQ: Profit from parallel FGT readout system development

HFT/IST/Specifications

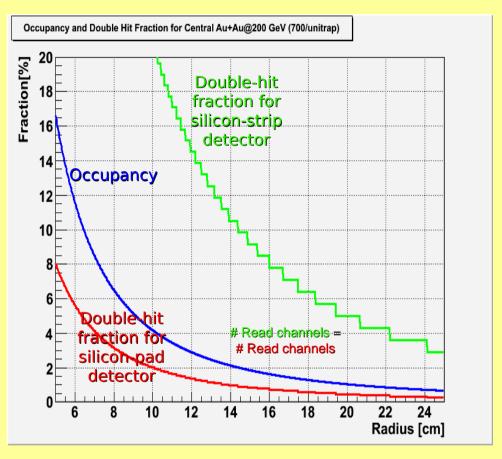


Radius	14 cm
Length	50 cm
Number of ladders	24
Number of hybrids	72
Number of sensors	144
Number of readout chips	864
Number of channels	110592
R-\phi resolution	172 μm
Z resolution	1811 μm

HFT/IST/Optimizing

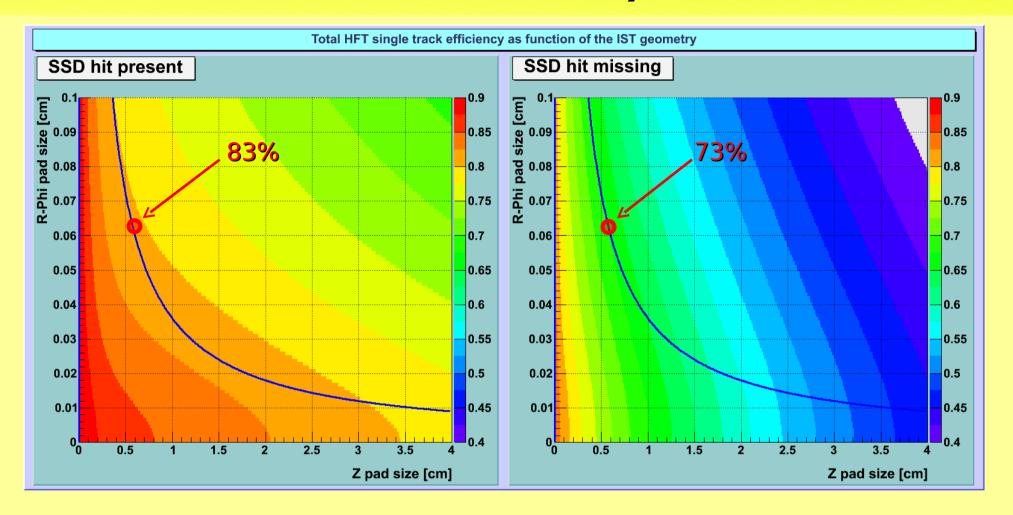


 Choice of radius of r=14cm yields optimized single track efficiency / Fairly insensitive to single track efficiency



- Silicon pad structure preferred over silicon strip layout to reduce amount of double-hit fraction in central Au-Au collisions at 200GeV CME (700 particles per unit rapidity)
- Occupancy for silicon pad layout is ~ 2% at r=14cm

HFT/IST/Efficiency

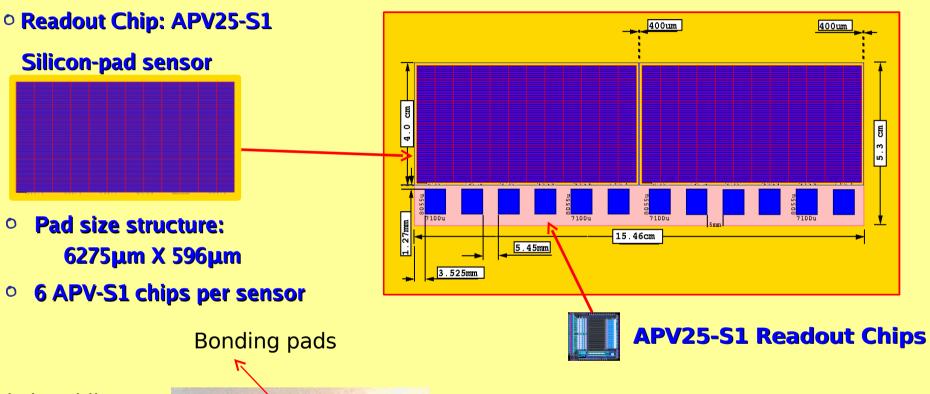


- 6 APV chips per sensor (768 channels) yields excellent efficiency with (without) SSD of 83% (73%)
- In comparison: 50% for TPC
- Efficiency relatively insensitive to changes in number of readout chips and layout of silicon pad sensors

HFT/IST/Technology

Module:

- 2 Silicon-pad sensors (Double-metal layer, AC coupled) 7.69cm X 4.0cm
- Light-weight Hybrid (Kapton-based / Carbon-fiber support material)



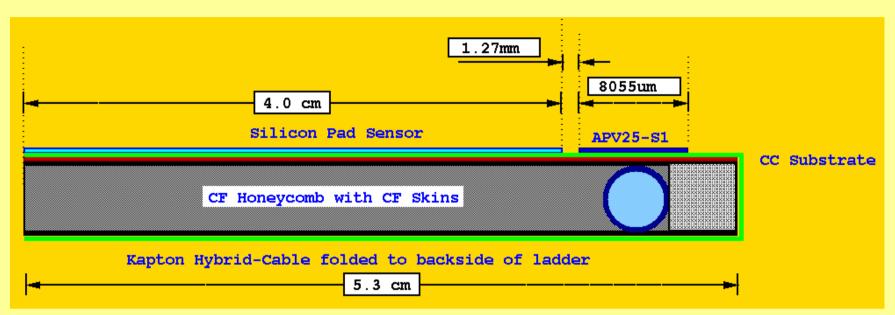
Metal signal lines

Silicon pads

(Example: PHOBOS silicon pad sensor)

Conservative technology
Multiple vendors (quote from Hamamatsu)
Expertise and labs at MIT-LNS

HFT/IST/Radiation_Length



Averaged radiation length
 over 5.3cm width: ~1.2% X₀

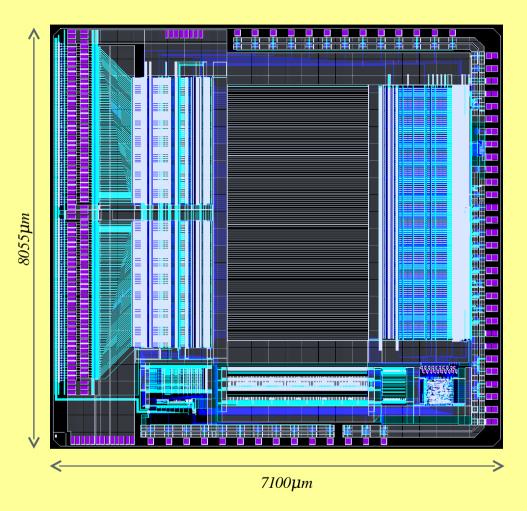
Readout chip	0.049%
CF honeycomb	0.060%
Cu traces hybrid/cable	0.18%
CF skin + glue	0.11%
CF skin + glue	0.11%
Carbon-Carbon core	0.23%
Silicon sensor	0.24%
Cooling water	0.05%
Al cooling tube	0.08%
Kapton	0.07%

HFT/IST/Prototypes



- 4 PHOBOS 512 channel pad sensors
- 16 APV25-S1 readout chips
- 75µm thick Kapton hybrid with 60cm long tail Assembled at MIT
- Wire bonded at BNL's Instrumentation Division
- 2 prototypes have been assembled
- 1 partially bonded prototype currently being tested
- Don Pinelli waiting for fine pitch bonding tools

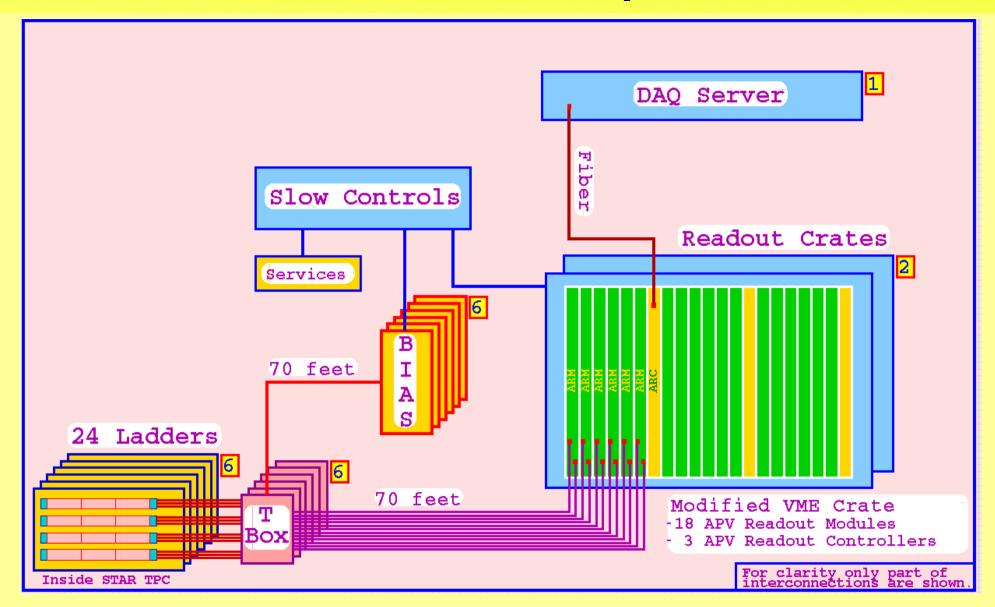
HFT/IST/Readout_Chip



- Developed for CMS (75000 in CMS tracker) and also used by COMPASS for triple-GEM detector readout
- 0.25μm CMOS
- 128 channels
- 40 MHz sampling rate
- 4µs analogue pipeline
- 11:1 Signal / Noise
- 0.3 Watt / chip
- Radiation hard

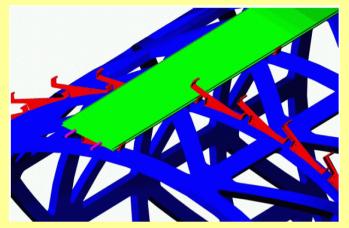
- 'Off-the shelf' readout chip: APV25-S1
- Used for STAR IST, FGT and pp2pp (1 readout system)!

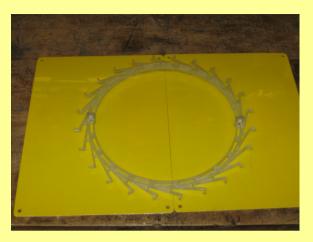
HFT/IST/Readout_System



First prototypes of ARM/ARC system ready May/June 2010.

HFT/IST/Mechanical_Support



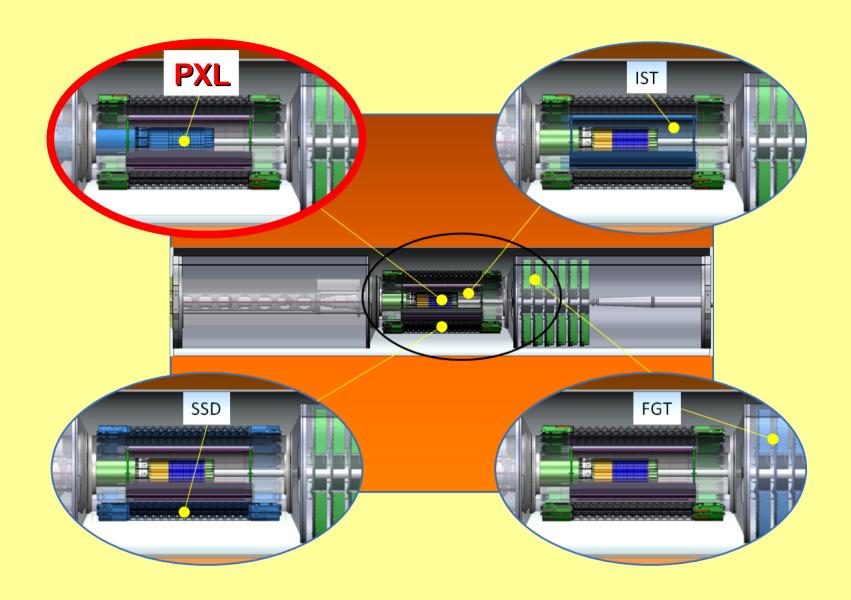




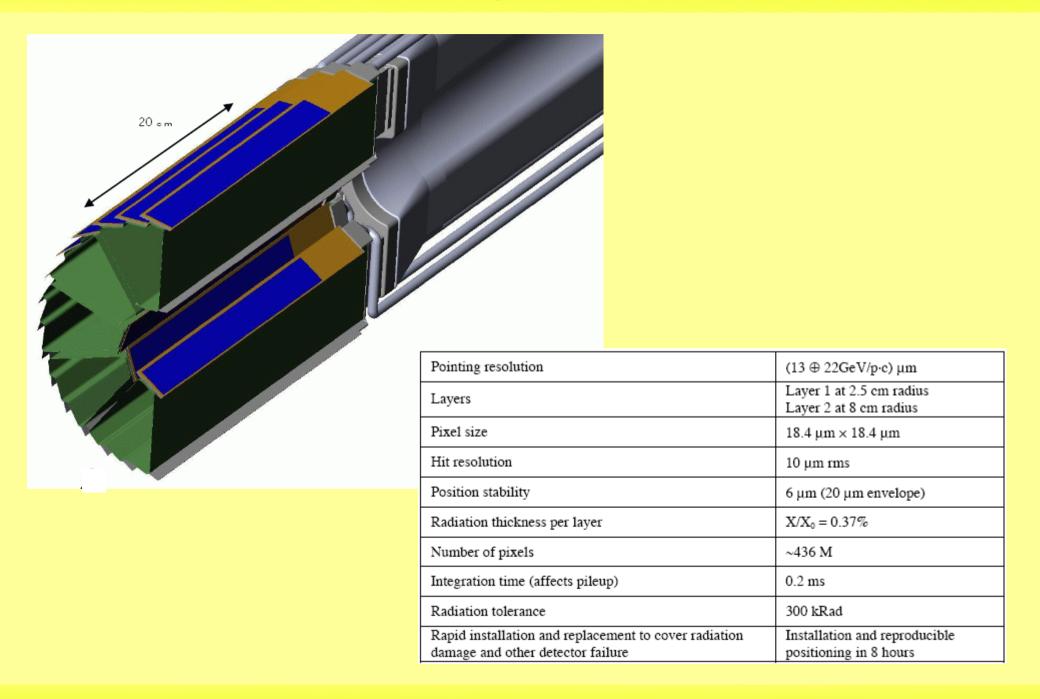


- Prototype ladder produced at LBNL: Carbon fiber honeycomb with carbon fiber skins (80cm / Current design is 50cm)
- 1 cooling channel
- Prototype ladder support rapid prototyped
- **Support mechanism: Click-in / Lock-in of ladders**

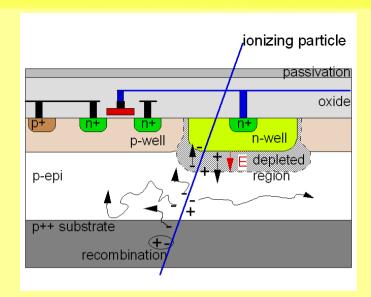
HFT/Detector/PXL



HFT/PXL/Specifications

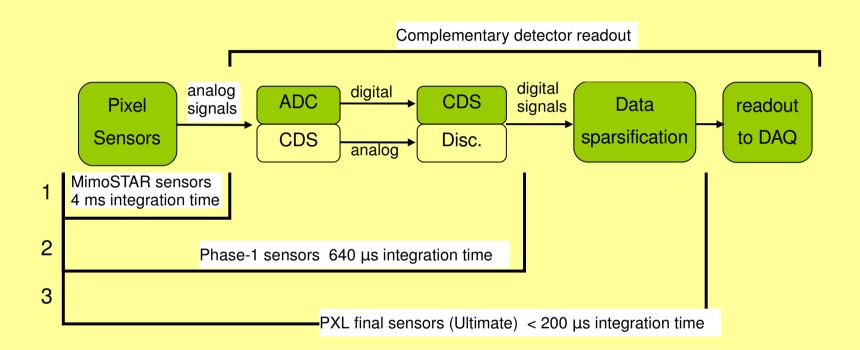


HFT/PXL/Technology



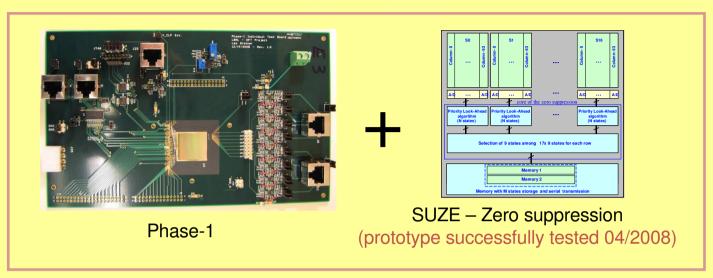
- Standard commercial CMOS technology
- Room temperature operation
- Sensor and signal processing are integrated in the same silicon wafer
- Signal is created in the low-doped epitaxial layer (typically ~10-15 µm) → MIP signal is limited to <1000 electrons
- Charge collection is mainly through thermal diffusion (~100 ns), reflective boundaries at p-well and substrate → cluster size is about ~10 pixels (20-30 µm pitch)
- 100% fill-factor
- Fast readout
- Proven thinning to 50 micron

HFT/PXL/Development



HFT/PXL/EndGame

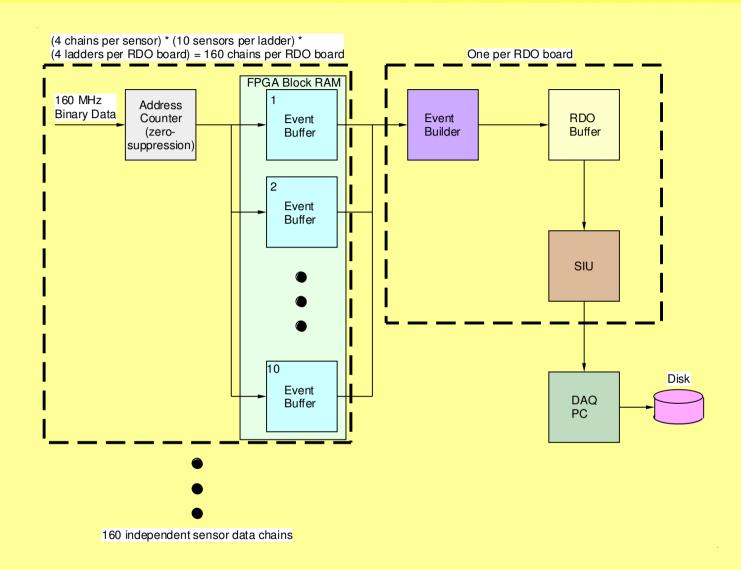
Final PXL Sensor



Last phase → **Ultimate sensor**

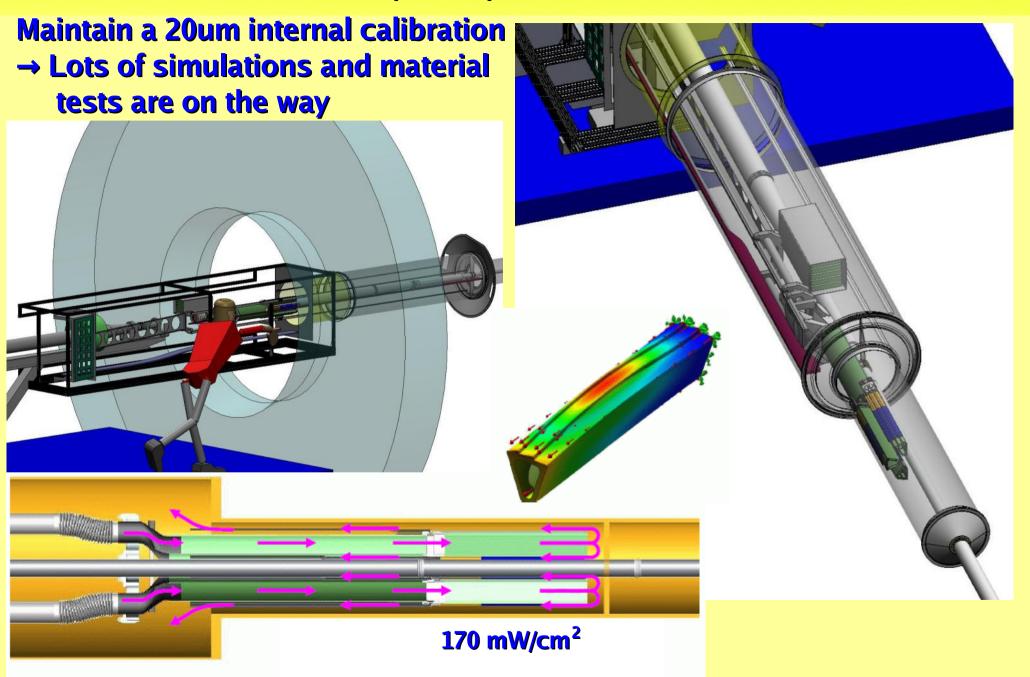
- Overall design is in progress and nearly complete.
- 18.4 m pixels have been chosen for enhanced radiation tolerance.
- Triggered detector system fitting into existing STAR infrastructure (Trigger, DAQ, etc.)
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC (1 kHz for DAQ1000).
- Have live time characteristics such that the Pixel detector is live whenever the TPC is live.
- Reduce the total data rate of the PXL detector to a manageable level (< TPC rate of ~1MB / event).

HFT/PXL/Readout

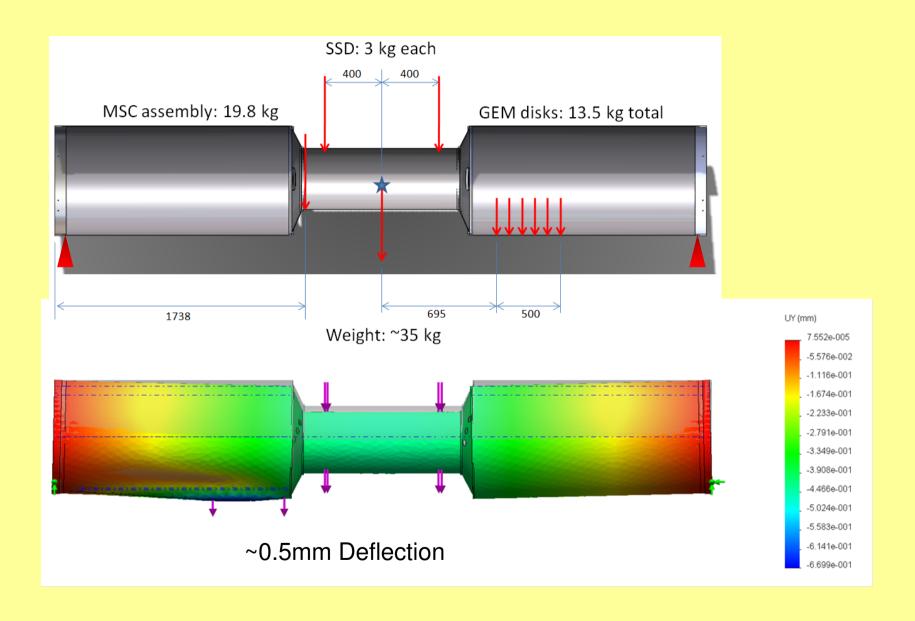


Easy to reconfigure FPGA firmware to adapt to final sensors

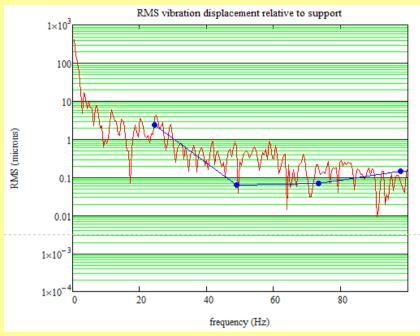
HFT/PXL/Mechanics

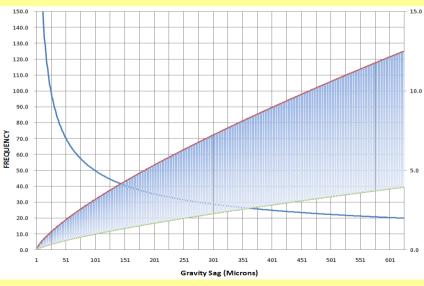


HFT/Support



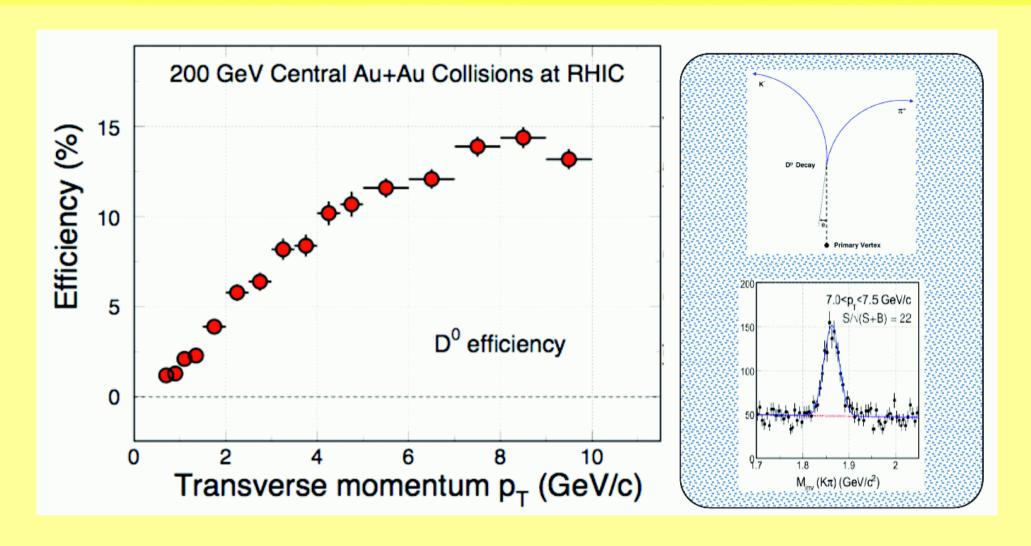
HFT/Stability





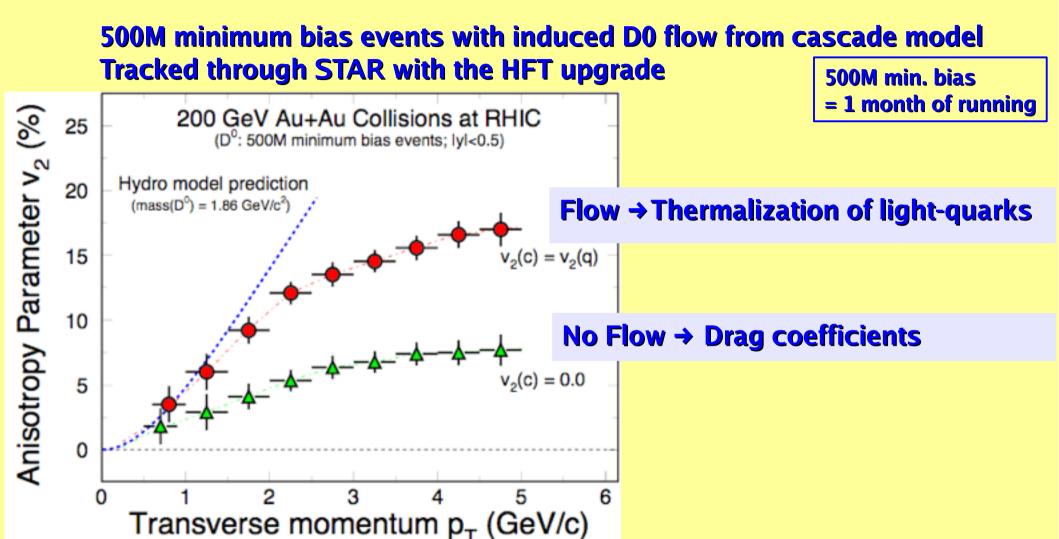
- Stability of IDS not critical for HFT unless Beam Constraint used (100μm)
- It is critical for FGT—
 FGT is intimately
 involved in design of IDS
- Gravity Sag can be used to project RMS Stability
- 0.5mm sag has $F_0 \sim 20$ Hz
- For Given PSD, Vibration is <10μm RMS
- IDS easily meets this requirement as designed

HFT/Performance



Because of the thin pixel layers the HFT will be able to measure down to $Pt \sim 0.5 \text{ GeV/c}$

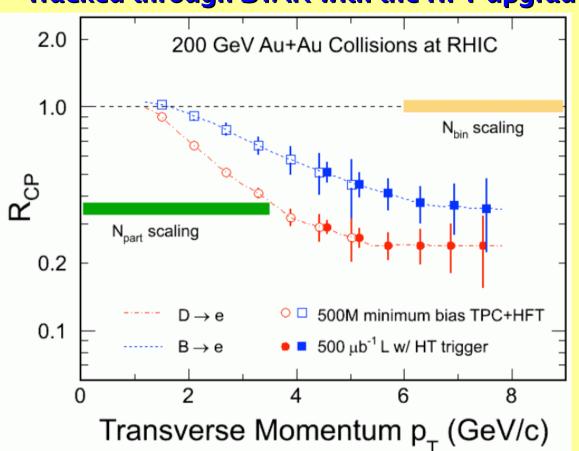
HFT/Flow



HFT will allow for precision measurements to address questions with respect to thermalization and in-medium effects

HFT/Suppression

500M minimum bias events from cascade model, D0 suppressed like light flavor Tracked through STAR with the HFT upgrade



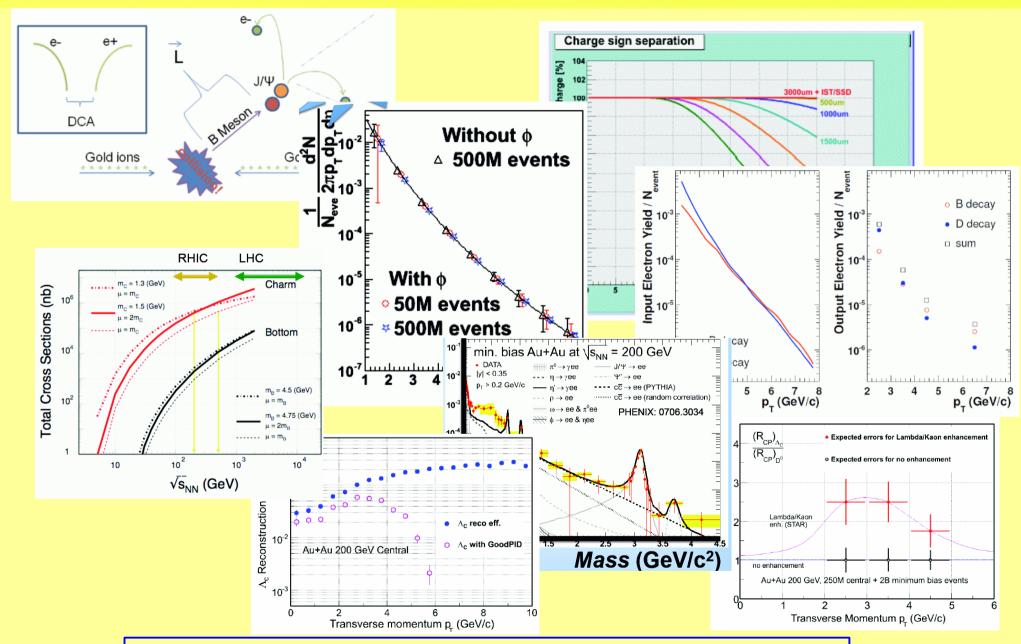
= 1 month of running

Significant contribution of electrons from bottom decay

Topological reconstruction of D0 necessary

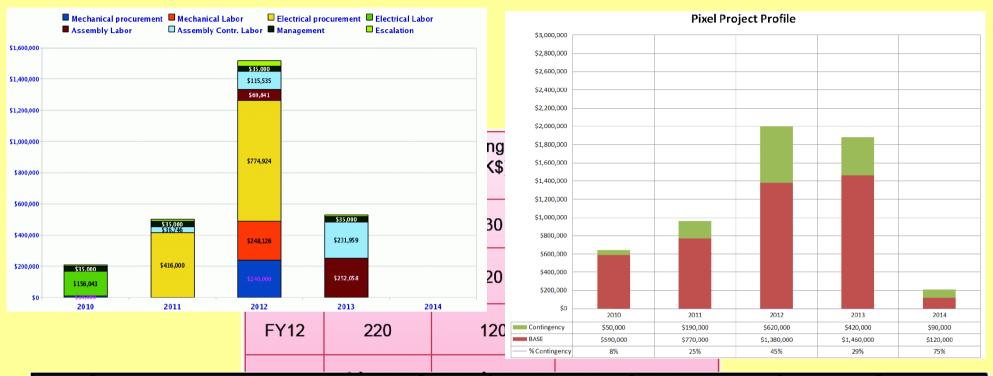
HFT will allow for precision charm measurements to address questions with respect to collisional and radiative effects

HFT/Whole_Lot_more



Waiting for the latest physics predictions before planning CD-2

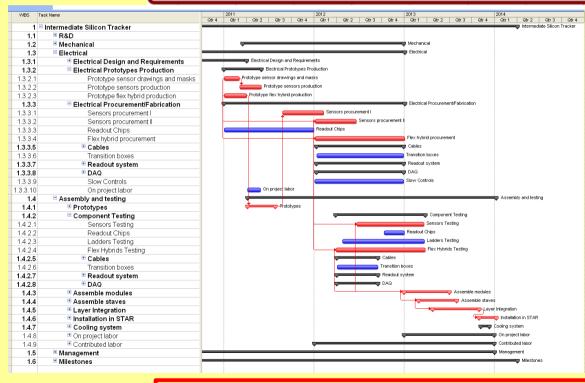
HFT/Funding



WBS	Title	Cost	Contingency %	Contingency \$	Low range	High Range
1.1	Proiect Management	1002	9%	90	1047	1124
1.2	Pixel	4780	32%	1540	5550	6859
1.3	Intermediate Silicon Tracker (IST)	2650	36%	960	3130	3946
1.4	Silicon Strip Detector (SSD)	660	44%	290	805	1052
1.5	Integration	1380	43%	600	1680	2190
	subtotal	10472	33%	3480	12212	15170
	Contributed Labor	2345		0	2345	2345
	Total Proiect Cost	12817		3480	14557	17515

HFT/Schedule

ID	mile stones			2010			2011				2012				2013				2014		
10	Time stories	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
1	Receive Prototype Sensors from IPHC						<	\Diamond													
2	Pixel Prototype Sector Design Complete																				
3	Prototype Insertion mechanism Testing Complete	ng							\diamond												
4	Receive final Ultimate Sensors from IPHC																				
5	Sector Assembly start																				
6	PXL detector available for insertion								\Diamond												



date	milestone
Q3	Review of board layout for ladder board and RDO
FY10	Start board (prototype) fabrication for both
Q2 FY11	Finish testing ladder board @BNL (digital event processing only). Finish testing RDO @BNL. Integrated testing @ Subatech for both boards
Q3 FY11	Develop slow controls and DAQ software
Q4 FY11	Produce full complement of boards
Q4 FY12	Move Full System to STAR for test
Q3 FV13	Install completed SSD in STAR

Planning to be ready for Run 14

HFT/Summary

HFT upgrade essential to extend STAR HI physics to heavy flavor sector

All components of HFT have been defined through Conceptional Design Report

All components of HFT are still on schedule, but slow funding is becoming an issue

Waiting for CD-1, preparing for CD-2/3